Joyen Benitto

SoC Design Engineer
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Research Vision

- Drive innovation in EDA and SoC design/verification methodologies
- Develop faster, more efficient, and reliable computing systems from embedded to cloud
- Develop reproducible, scalable and open-source research
- Bridge the gap between academic research and industry applications
- Contribute to teaching and mentoring in computer architecture

Experience

SoC Design Engineer Jun'24 – Present
InCore Semiconductors, IIT Madras Research Park

- Architected, developed and maintained RISC-V SoC generator platform and associated methodologies
  - Speced and developed the design rule checks and architecture specification schemas
  - SoC IP integration (Generation of the soc_top.v)
  - FPGA emulation support
  - Ready to use software collateral generation (baremetal, zephyr BSPs and Eclipse IDE)
  - Software smoke test for register accesses
  - SoC level documentation
  - All the SoCs shipped to customers are generated using our SoC generator platform
- Architected DDSL (Device Drivers Specification Language), a DSL for device driver specification and generation
- Architected Device Manager, a scalable framework for IP management that automates:
  - Verilog to Bluespec SystemVerilog wrapper generation
  - Test infrastructure and documentation generation
  - Third-party IP integration and maintenance
- Speced, developed and maintained Pinmux Generator, a tool that enables real-time reconfiguration of pin assignments to optimize packaging costs and increase pin functionality
- Managed a tiny team of interns and engineers who contribute to our SoC generator platform and SW collateral generation
- Occasionally, I participate in customer evaluation calls and also present demos of our SoC generator platform to potential customers
- Worked under the supervision of Dr. Neel Gala (CTO, InCore Semiconductors)

Intern Jun'23 – May'24
InCore Semiconductors, IIT Madras Research Park

- Contributed to Azurite, a configurable RISC-V heterogeneous core generator platform
- Initiated the SoC Generator project
- Worked under the supervision of Dr. Neel Gala (CTO, InCore Semiconductors)

Research Contributor Oct'23 – Dec'23
Centre for Heterogeneous and Intelligent Processing Systems, Bangalore

- Contributed to the development of PARISCV, a RISC-V application profiler for custom instruction set optimization
- Research published at OSCAR'24, focusing on hardware-software co-design methodologies
- Conducted research under Dr. Madhura Purnaprajna's supervision

Academic Appointments

Teaching Assistant, RISC-V Architecture Oct'23 – Dec'23
Department of ECE, PES University

- Assisted Prof. Mahesh Awati in teaching RISC-V Architecture
- Conducted tutorial sessions and provided technical guidance

Education

B.Tech in Electronics and Communication Engineering Jun'20 – Jun'24
PES University

- **Research Focus:** EDA, Computer Architecture, Hardware-Software Co-design

Publications

[1] **Benitto, J.**, et al. "PARISCV: A Profiler for Application-Specific Acceleration on RISC-V"
Open Source Computer Architecture Research Conference (OSCAR'24)

[2] **Benitto, J.**, et al. "Enhancing Micro-Strip Patch Antenna Design for HFSS Using a Python Package -'AntGen'."
IEEE Microwave, Antennas and Propagation Conference (MAPCON'23)

Technical Expertise

- **Hardware Description Languages:** SystemVerilog, Verilog, Bluespec SystemVerilog
- **Programming Languages:** Python, C, C++, Rust, Haskell, CUDA
- **Development Tools:** Git, Linux, Docker, CI/CD

Academic Leadership

Co-Founder, Hyperthrd Computer Architecture Community Oct'23 – Present

- Founded and led a student-driven research community focused on computer architecture
- Organize technical discussions and research presentations

Technical Mentor, Hackerspace Sep'22 – Dec'23

- Mentored students in hardware development and computer architecture
- Conducted workshops on RISC-V architecture and hardware design

Talks and Lectures

- **A brief introduction to SoC design and automation methodologies**
  Presented at Hyperthrd Community Meetup, Dec 2023
- **Understanding RISC-V microarchitecture the simplest way**
  Workshop at PES University, Nov 2023
- **Understanding Compilers, linkers and loaders with RISC-V GCC toolchain**
  Building from C to binary using RISC-V GCC, Hackerspace Workshop, Oct 2023
- **Coolio with CUDA**
  Introduction to CUDA and Data-level parallelism, PES University, Sep 2023
- **NVIDIA's Fermi: The First Complete GPU Computing Architecture**
  Computer Architecture Seminar, PES University, Aug 2023
- **Data-level Parallelism and SIMD Architectures**
  Guest lecture, Advanced Computer Architecture course, Jul 2023

Blogs and Articles

- ***A Pragmatic Left-Shift Methodology***
  Tools & Techniques for Exploring and Building Domain-Specific SoCs
  `https://www.joyenbenitto.com/posts/left_shift_dsa`
- ***IP-Xact: The Hero We Need, the Villain We Deserve?***
  An analysis of IP-XACT standard for SoC design automation
  `https://www.joyenbenitto.com/posts/ipxact_the_hero_villain_blog`